Listing of the Claims:

Below is a listing of all claims using a strikethrough and underlining to show changes.

1. (currently amended) An automatic timing analyzer for determining a propagation delay time of an electronic circuit ~~of testing electronic circuits~~ comprising:

a first timer for performing a coarse ~~timing~~ measurement of ~~an electronic circuit~~ propagation delay time;

a second timer for performing a fine ~~timing~~ measurement of ~~the electronic circuit~~ of propagation delay time; and

storage means for storing timing measurements of the first and second timers.

2. (Original) The automatic timing analyzer recited in claim1, wherein the electronic circuits are integrated circuits and the timing analyzer is a component of a Built In Self Test (BIST) system on an integrated circuit.

3. (Original) The automatic timing analyzer recited in claim 2, wherein the BIST system includes separately controlled delay elements for controlling timing of output signals for said first and second timers.

4. (Original) The automatic timing analyzer recited in claim 3, wherein the delay elements are controlled by individual control words.

5. (Original) The automatic timing analyzer recited in claim 4, wherein the control words are generated from a bank of binary counters.

6. (Original) The automatic timing analyzer recited in claim 5, wherein relative timing of output signals is adjusted by incrementing or decrementing respective counters in the bank of binary counters.

7. (Original) The automatic timing analyzer recited in claim 5, wherein a set of control words are stepped through by the bank of binary counters.

8. (currently amended) An integrated circuit having a Built In Self Test (BIST) system which includes a first timer for performing a coarse ~~timing~~ propagation delay time measurement of the integrated circuit, a second timer for performing a fine ~~timing~~ propagation delay time measurement of the integrated circuit, and storage means for storing ~~timing~~ measurements of the first and second timers.

9. (Original) The integrated circuit recited in claim 8, wherein the BIST system is used to test effects of timing skews between multiple stimuli.

10. (Original) The integrated circuit recited in claim 9, wherein all possible combinations of a plurality of timing signals and a plurality of timing variations are tested.

11. (currently amended) A method of testing electronic circuits comprising the steps of:

performing a coarse ~~timing~~ propagation delay time measurement of an electronic circuit;

performing a fine ~~timing~~ propagation delay time measurement of the electronic circuit; and

storing the coarse and fine timing measurements.

12. (Original) The method of testing recited in claim 11, further comprising the step of controlling timing signals for said coarse and fine timing measurements.

13. (Original) The method of testing recited in claim 12, wherein the step of controlling is performed using individual control words.

14. (Original) The method of testing recited in claim 13, further comprising the step of generating the individual control words with a bank of binary counters.

15. (Original) The method of testing recited in claim 14, further comprising the step of incrementing or decrementing respective counters in the bank of binary counters to adjust relative timing for said coarse and fine testing measurements.

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